IN THE CLAIMS:

Please amend the claims as set forth below.

1. (Currently Amended) An apparatus comprising:

a first storage location configured to store a first indication, the first storage location addressable by a first instruction defined by a processor architecture, wherein the first indication is an enable indication defined in the processor architecture to indicate whether or not a first mode defined in the processor architecture is to be enabled;

a second storage location configured to store a second indication, the second storage location addressable by a second instruction defined by the processor architecture, the second instruction being different from the first instruction, and wherein the second indication is a paging indication defined in the processor architecture to indicate whether or not paging is enabled;

a third storage location configured to store a mode indication, the mode indication indicative of whether or ~~not a first~~ not the first mode ~~defined in the processor architecture~~ is active, and wherein the first mode permits an address size greater than 32 bits and an operand size greater than 32 bits; and

a processor configured to generate the mode indication responsive to the first indication and the second indication.

2-3. (Cancelled)

4. (Currently Amended) The apparatus as recited in ~~claim 3 wherein~~ claim 1 wherein the mode indication indicates that the first mode is active if the enable indication is in an

enabled state and the paging indication indicates that paging is enabled.

5. (Currently Amended) The apparatus as recited in ~~claim 3 wherein~~ claim 1 wherein the processor is configured to check a status of one or more indications including the enable indication and the paging indication when changing one of the one or more indications to ensure that the change is permitted by the processor architecture.

6. (Previously Presented) The apparatus as recited in claim 5 wherein the processor is configured to signal an exception instead of changing the one of the one or more indications if the change is not permitted.

7. (Original) The apparatus as recited in claim 5 wherein, if the enable indication is changed from a disabled state to an enabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted.

8. (Original) The apparatus as recited in claim 5 wherein, if the enable indication is changed from an enabled state to a disabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted.

9. (Original) The apparatus as recited in claim 5 wherein, if the paging indication is changed from indicating that paging is disabled to indicating that paging is enabled, the change is not permitted if the enable indication is in an enabled state and another indication indicates that physical address extension is disabled.

10. (Original) The apparatus as recited in claim 5 wherein the one of the one or more indications is an indication of whether or not physical address extension is enabled, and wherein the change is not permitted if the enable indication is in an enabled state.

11. (Original) The apparatus as recited in claim 1 further comprising a fourth storage location configured to store a segment selector identifying a segment descriptor including a first operating mode indication and a second operating mode indication, and wherein

the processor is configured to generate an operating mode responsive to the mode indication, the first operating mode indication, and the second operating mode indication.

12. (Original) The apparatus as recited in claim 1 wherein the first storage location is located within a first register defined by the processor architecture, and wherein the second storage location is located within a second register defined by the processor architecture.

13. (Original) The apparatus as recited in claim 12 wherein the third storage location is located within the first register.

14. (Original) The apparatus as recited in claim 12 wherein the first register and the second register are incorporated within the processor.

15. (Original) The apparatus as recited in claim 14 further comprising a circuit coupled to the first register and the second register, wherein the circuit is configured to generate the mode indication for storage in the third storage location.

16. (Original) The apparatus as recited in claim 1 wherein the processor implements the processor architecture.

17. (Original) The apparatus as recited in claim 1 wherein the processor emulates the processor architecture.

18. (Original) The apparatus as recited in claim 17 wherein the processor executes interpreter software for interpreting instructions defined in the processor architecture.

19. (Original) The apparatus as recited in claim 17 wherein the processor executes translator software for translating instructions defined in the processor architecture to instructions executable by the processor.

20. (Original) The apparatus as recited in claim 17 wherein the processor executes a combination of: (i) interpreter software for interpreting instructions defined in the processor architecture; and (ii) translator software for translating instructions defined in the processor architecture to instructions executable by the processor.

21. (Currently Amended) A processor comprising:

a first register configured to store a first indication, the first register addressable by a first instruction, wherein the first indication is an enable indication defined in a processor architecture of the processor to indicate whether or not a first mode defined in the processor architecture is to be enabled;

a second register configured to store a second indication, the second register addressable by a second instruction different from the first instruction, wherein the second indication is a paging indication defined in the processor architecture to indicate whether or not paging is enabled; and

a circuit coupled to the first register and the second register, wherein the circuit is configured to generate a mode indication responsive to the first indication and the second indication, wherein the mode indication is indicative of whether or ~~not a first~~ not the first mode ~~defined in a processor architecture of the processor~~ is active, and wherein the first mode permits an address size greater than 32 bits and an operand size greater than 32 bits, and wherein the circuit is configured to store the mode indication in a location addressable by an instruction.

22-23. (Cancelled)

24. (Currently Amended) The processor as recited in ~~claim 23 wherein~~ claim 21 wherein the mode indication indicates that the first mode is active if the enable indication is in an enabled state and the paging indication indicates that paging is enabled.

25. (Currently Amended) The processor as recited in ~~claim 23 wherein~~ claim 21 wherein the processor is configured to check a status of one or more indications including the enable indication and the paging indication when changing one of the one or more indications to ensure that the change is permitted by the processor architecture.

26. (Previously Presented) The processor as recited in claim 25 wherein the processor is configured to signal an exception instead of changing the one of the one or more indications if the change is not permitted.

27. (Original) The processor as recited in claim 25 wherein, if the enable indication is changed from a disabled state to an enabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted.

28. (Original) The processor as recited in claim 25 wherein, if the enable indication is changed from an enabled state to a disabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted.

29. (Original) The processor as recited in claim 25 wherein, if the paging indication is changed from indicating that paging is disabled to indicating that paging is enabled, the change is not permitted if the enable indication is in an enabled state and another indication indicates that physical address extension is disabled.

30. (Original) The processor as recited in claim 25 wherein the one of the one or more indications is an indication of whether or not physical address extension is enabled, and wherein the change is not permitted if the enable indication is in an enabled state.

31. (Original) The processor as recited in claim 21 further comprising a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication and a second operating mode indication, and wherein the circuit is configured to generate an operating mode responsive to the mode indication, the

first operating mode indication, and the second operating mode indication.

32. (Original) The processor as recited in claim 21 wherein the mode indication is also stored in the first register.

33. (Currently Amended) A method comprising:

storing a first indication in a first storage location addressable by a first instruction, wherein the first indication is an enable indication defined in a processor architecture to indicate whether or not a first mode defined in the processor architecture is to be enabled;

storing a second indication in a second storage location addressable by a second instruction, wherein the second indication is a paging indication defined in the processor architecture to indicate whether or not paging is enabled;

generating a mode indication indicative of whether or ~~not a first~~ not the first mode ~~defined in a processor architecture~~ is active, the generating responsive to the first indication and the second indication, wherein the first mode permits an address size greater than 32 bits and an operand size greater than 32 bits; and

storing the mode indication in a third addressable storage location.

34-35. (Cancelled)

36. (Currently Amended) The method as recited in ~~claim 35 wherein~~ claim 33 wherein the generating comprises generating the mode indication to indicate that the first mode is active if the enable indication is in an enabled state and the paging indication indicates that paging is enabled.

37. (Currently Amended) The method as recited in ~~claim 35 further~~ claim 33 further comprising checking a status of one or more indications including the enable indication and the paging indication when changing one of the one or more indications to ensure that the change is permitted by the processor architecture.

38. (Previously Presented) The method as recited in claim 37 further comprising signalling an exception instead of changing the one of the one or more indications if the change is not permitted.

39. (Original) The method as recited in claim 37 wherein the checking comprises, if the enable indication is changed from a disabled state to an enabled state, checking that the paging indication indicates that paging is disabled for the change to be permitted.

40. (Original) The method as recited in claim 37 wherein the checking comprises, if the enable indication is changed from an enabled state to a disabled state, checking that the paging indication indicates that paging is disabled for the change to be permitted.

41. (Original) The method as recited in claim 37 wherein, if the paging indication is changed from indicating that paging is disabled to indicating that paging is enabled, the change is not permitted if the enable indication is in an enabled state and another indication indicates that physical address extension is disabled.

42. (Original) The method as recited in claim 37 wherein the one of the one or more indications is an indication of whether or not physical address extension is enabled, and wherein the change is not permitted if the enable indication is in an enabled state.

43. (Original) The method as recited in claim 33 further comprising generating an operating mode responsive to the mode indication, a first operating mode indication, and a second operating mode indication, wherein the first operating mode indication and the second operating mode indication are included in a segment descriptor identified by a segment selector stored in a fourth storage location.

44-49. (Cancelled)

50. (Previously Presented) A processor comprising:

a first register configured to store an enable indication indicative of whether or not a first mode is to be enabled, the first register addressable by a first instruction;

a second register configured to store a paging indication indicative of whether or not paging is enabled, the second register addressable by a second instruction different from the first instruction; and

a circuit coupled to the first register and the second register, wherein the circuit is configured to generate a mode indication responsive to the enable indication and the paging indication, wherein the mode indication is indicative of whether or not a first mode of the processor is active, the first mode permitting an address size greater than 32 bits and an operand size greater than 32 bits, and wherein the circuit is configured to store the mode indication in a location addressable by an instruction.

51. (Previously Presented) The processor as recited in claim 50 wherein the mode indication indicates that the first mode is active if the enable indication is in an enabled state and the paging indication indicates that paging is enabled.

52. (Previously Presented) The processor as recited in claim 50 wherein the processor is configured to check a status of one or more indications including the enable indication and the paging indication when changing one of the one or more indications to ensure that the change is permitted.

53. (Previously Presented) The processor as recited in claim 52 wherein the processor is

configured to signal an exception instead of changing the one of the one or more indications if the change is not permitted.

54. (Previously Presented) The processor as recited in claim 52 wherein, if the enable indication is changed from a disabled state to an enabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted.

55. (Previously Presented) The processor as recited in claim 52 wherein, if the enable indication is changed from an enabled state to a disabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted.

56. (Previously Presented) The processor as recited in claim 52 wherein, if the paging indication is changed from indicating that paging is disabled to indicating that paging is enabled, the change is not permitted if the enable indication is in an enabled state and another indication indicates that physical address extension is disabled.

57. (Previously Presented) The processor as recited in claim 52 wherein the one of the one or more indications is an indication of whether or not physical address extension is enabled, and wherein the change is not permitted if the enable indication is in an enabled state.

58. (Previously Presented) The processor as recited in claim 50 further comprising a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication and a second operating mode indication, and wherein the circuit is configured to generate an operating mode responsive to the mode indication, the first operating mode indication, and the second operating mode indication.

59. (Previously Presented) The processor as recited in claim 50 wherein the mode indication is also stored in the first register.

60. (Previously Presented) A computer system comprising the processor as recited in

claim 50 and a device configured to communicate between the computer system and another computer system.

61. (Previously Presented) The computer system as recited in claim 60 wherein the device comprises a modem.

62. (Previously Presented) The computer system as recited in claim 60 wherein the device comprises a network interface circuit.

63. (Previously Presented) A computer system comprising the processor as recited in claim 21 and a device configured to communicate between the computer system and another computer system.

64. (Previously Presented) The computer system as recited in claim 63 wherein the device comprises a modem.

65. (Previously Presented) The computer system as recited in claim 63 wherein the device comprises a network interface circuit.

66. (Currently Amended) A computer readable medium storing a plurality of instructions which, when executed:

responsive to a first instruction, update a first storage location configured to store a first indication, wherein the first indication is an enable indication indicative of whether or not a first mode defined in a processor architecture is to be enabled;

responsive to a second instruction, update a second storage location configured to store a second indication, wherein the second indication is a paging indication indicative of whether or not paging is enabled;

generate a mode indication responsive to the first indication and the second indication, the mode indication indicative of whether or ~~not a first~~ not the first mode is active in a processor, wherein the first mode permits an address size greater than 32 bits and an operand size greater than 32 bits; and

update a third storage location configured to store the mode indication.

67. (Previously Presented) The computer readable medium as recited in claim 66 wherein the plurality of instructions emulate the first instruction and the second instruction.

68. (Previously Presented) The computer readable medium as recited in claim 66 wherein the plurality of instructions are executed in place of the first instruction and the second instruction.

69-70. (Cancelled)

71. (Currently Amended) The computer readable medium as recited in ~~claim 70 wherein~~ claim 66 wherein the mode indication indicates that the first mode is active if the enable indication is in an enabled state and the paging indication indicates that paging is enabled.